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Phase compensation of gate tracked RF power amplifier for supply modulation applications

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Summary

A novel method for reducing phase variations in a supply modulated amplifier is developed. For supply modulated (envelope tracked) PA's the drain voltage is varied according to the input signal to enhance efficiency. To flatten the gain, the gate voltage may also be modulated. The presented configuration including an additional "ghost" transistor significantly reduce the AM-PM nonlinearities. The additional transistor is only connected by the gate and have no current in the drain. The gate voltage of the compensating transistor is varied opposite of the original gate voltage. By comparison with an optimized class inverse F PA, the compensated version shows AM-PM reduction from 48 to 26.5 degrees over a wide range of V_{gs} and V_{ds}.

1. Introduction

This paper deals with GaN on SiC RF Power Amplifiers and linearization hereof. It is well known that essential properties of an RF Power amplifier as efficiency, bandwidth, and linearity is a trade-off which of them to prioritize in each case. There are several methods to enhance each of the mentioned parameters [1]. The initial motivation for the development described in this paper is the supply modulation method for efficiency enhancement of power amplifiers operating in high back-off. For supply modulated amplifiers also gate modulation is used to compensate and flatter the gain [1] [2]. Ideally the properties of the transistor amplifier do not vary (gain and phase) with drain voltage. This is not the case with GaN PAs, and several methods may be introduced to compensate the nonlinearities, as gate tracking [3] and digital- and analog predistortion [1]. By varying the gate voltage, the gain may be compensated, the phase is not easily controlled by this method. To control the phase additional control is necessary, as in [4] where the gate of two cascaded amplifiers are controlled. It is desirable to compensate the phase nonlinearities of the amplifier, both as gate voltage, drain voltage and RF power input varies. By embedding nonlinear component(s) in the amplifier to compensate the phase variation, the need of external control signal is eliminated. At least the complexity of external control signal is reduced.

2. Nonlinear gate capacitance

We consider all phase variations in a power amplifier related to nonlinear behavior of voltage dependent capacitances. By simulation the gate capacitance for GaN transistor CG2H40010F from (1). We observe C_{ds} and C_{gd} are dependent of V_{ds} and V_{gs}, C_{gs} show low dependence of $V_{ds.}$

$$C_{GS} = \frac{|y_{22}+y_{22}|^2}{\omega \cdot Im\,(y_{11}+y_{12})} \qquad (1).$$

3. Design of compensated Power Amplifier

The goal is to design a 10W 2.1GHz power amplifier for supply modulation applications. Transistor used for the design is CG2H40010F. To eliminate the phase variation due to variation of $C_{gs(q1)}$ the gate capacitance of another transistor is placed in parallel. The sum $C_{gs(q1)} + C_{gs(q2)}$ is constant if the transistors are equal, and the gate voltages are opposite symmetrical of the middle point of the capacitance trajectory (fig. 5). The gate voltage of the main transistor Vg and the compensating "ghost" transistor V_{gg}. If we assume the capacitance is symmetrical around V_g=-2.5V, V_{gg}=-5- V_g .
The actual CG2H40010F transistors are packaged and includes the parasites as in fig. 2, mainly caused by the bonding wires. Still phase compensation is achievable. To optimize the compensation effect over Vgs and applied input power, a transmission line is inserted between the gates of Q1 and Q2. The electrical length is found by optimization in the simulator. To evaluate the method, source-pull and load pull-blocks were used for simulation. The source-pull tuned up to 3rd harmonic to perform optimal class inverted F. The amplifier tuned to maximum P.A.E. @ 2.1GHz, Pout>40dBm and maximum gain. This procedure was performed for two versions of the amplifier, the first one a conventional single transistor and the other with compensating transistor. The compensated version was in addition to P.A.E and Pout optimized in term of phase variation over V_{gs} = [-2.8, -2.2]V, with Pin = [0, 30]dBm.

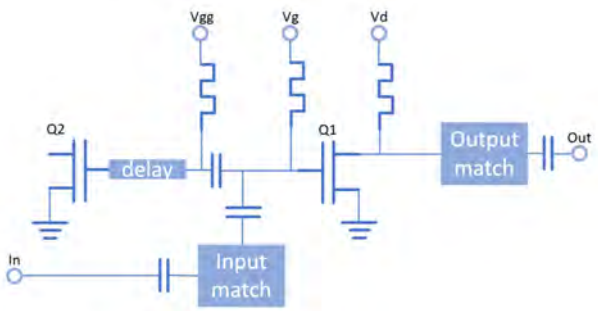

Figure 1. 10W 2.1GHz class inverted F power amplifier /w gate capacitance compensating transistor.

4. Results

TABLE I. SIMULATION OF 2.1GHZ, 10W PA

Difference	Simulated class inverted class F PA with/without compensation		
	Parameter / range	*One transistor*	*Compensated*
-9	P.A.E [%]	86.3	74.6
-0.2	Pout max [dBm]	40.6	40.4
-0.2	G [dB] @ 25dBm input	15.6	15.4
-20.8	$Bandwidth_{3dB}$ [%]	60.2	39.4
-18	Δθ [deg] @ Vds=28V, Vgs = [-2.8, -2.2V], Pin = [0, 30]dBm	28.1	10.1
-21.5	Δθ [deg] @ Vds=[7, 28]V, Vgs = [-2.8, -2.2]V, Pin = [0, 30]dBm	48.0	26.5

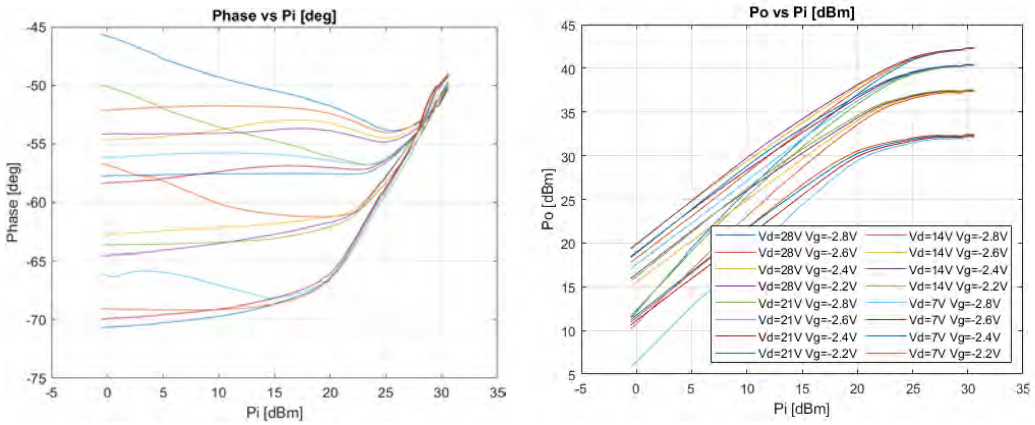

Figure 2. Measured PA /w gate capacitance compensation, Pout V_{ds}=7, 14, 21, 28V, V_{gs} = [-2.8, -2.2]V, Pin = [0, 30]dBm

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